REMARKS

Claims 1–18 are pending in the present application. Claims 8–18 have been withdrawn from consideration.

Reconsideration of the claims is respectfully requested.

35 U.S.C. § 112, Second Paragraph (Definiteness)

Claim 6 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. This rejection is respectfully traversed.

The Office Action objects to the recitation in claim 6 of "mounting adjacent packaged integrated circuits in contact with each other." The portions of the specification cited in the Office Action teach that integrated circuit die are mounted on a lead frame for packaging with a separation equal to a kerf or saw width. After encapsulation, the individual integrated circuit die are singulated (separated) prior to mounting on a printed circuit board. Accordingly the integrated circuit die, while separated on the lead frame during encapsulation, are unconnected after completion of packaging and may be mounted in contact with each other on a printed circuit board.

Therefore, the rejection of claim 6 under 35 U.S.C. § 112, second paragraph has been overcome.

35 U.S.C. § 103 (Obviousness)

Claims 1–5 and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,894,707 to *Yamawaki et al* in view of U.S. Patent No. 6,300,169 to *Weiblen et al*, U.S. Patent No. 6,252,252 to *Kunii et al* and further in view of U.S. Patent No. 6,255,741 to *Yoshihara et al* and U.S. Patent No. 6,171,879 to *Chan et al*. This rejection is respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP § 2142.

Independent claim 1 recites forming a linear photosensor array from a plurality of packaged photosensor integrated circuits mounted with photosensors in alignment on a printed circuit board with at least some leads soldered. Such a feature is not shown or suggested by the cited references. *Yamawaki et al* teaches a single array of photosensors within a single integrated circuit for a video recording device, but does not suggest that multiple integrated circuits be mounted on a single printed circuit board with the photosensor arrays aligned. The cited portion of *Weiblen et al* depicts a lead grid with an array of lead frames for mass-production, concurrent packaging of multiple pressure sensor integrated circuits, but does not teach or suggest any photosensors or that the pressure sensors are subject to any particular effort

at intentional alignment when mounted on the lead frame. *Weiblen et al*, Figure 1, column 2, lines 44–53. *Kunii et al* teaches an integrated circuit with a light emitting element, but does not suggest mounting a plurality of such integrated circuits on a printed circuit board with the light emitting elements in alignment. None of the cited references teach or suggest that a plurality of integrated circuits each having a photosensor array be mounted in a printed circuit board with the photosensors aligned.

Independent claim 1 also recites that at least some leads for each integrated circuit are soldered to the circuit board. In an exemplary embodiment, the integrated circuits are mounted on lead frames (using a lead frame grid and then singulating), preferably packaged (encapsulated), then mounted on the printed circuit board with at least leads on one side being soldered. Such a feature is not shown or suggested by the cited references. None of the cited references teaches mounting integrated circuit die on lead frames, then mounting the die and lead frames on a circuit board with photosensors in alignment and soldering at least some of the leads.

Claim 2 recites additional details of packaging the integrated circuit die, including wire bonding and encapsulation, prior to mounting the packaged integrated circuits on the circuit board with the photosensors in alignment. Such a feature is not shown or suggested by the cited references.

Claims 3 and 4 recite details of packaging the integrated circuits so that the photosensors remain exposed, by utilizing a mold with a surface contacting the photosensor array surface. Such a feature is not shown or suggested by the cited references.

Claim 5 recites that the integrated circuit die are mounted on the lead frame grid with a spacing equal to the kerf for the singulation saw separating the integrated circuits after encapsulation. As a result, the packaged photosensors may be mounted on the circuit board in contact, or with a separation of less than 10 microns, so that the array scans a line sufficiently complete that existing interpolation techniques can supply any missing pixels. Such a feature is not shown or suggested by the cited references. *Yoshihara et al* teaches singulation of integrated circuit die within a wafer utilizing a saw, but does not teach or suggest intentionally mounting integrated circuit die on a lead frame or the like with a spacing equal to the singulation kerf.

Claim 7 recites soldering only leads on one side of the packaged integrated circuit die, leaving the other leads in floating contact to facilitation adjustment. Such a feature is not shown or suggested by the cited references. At the time of the invention claimed herein, the subject application and U.S. Patent No. 6,171,879 to *Chan et al* were both owned by, and both subject to an obligation of assignment to, STMICROELECTRONICS, INC.

Therefore, the rejection of claims 1–5 and 7 under 35 U.S.C. § 103 has been overcome.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***dvenglarik@davismunck.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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